Modeling, Control, and Simulation of a Switched Amplifier Configured as a Common-Emitter Voltage-Variable Gain

José M. Campos-Salazar
jcampossalazar@gmail.com

***Abstract*—In this paper, a topology of a switched amplifier configured as a common-emitter voltage variable gain amplifier controlled by a nonlinear hysteresis controller is proposed. The proposed topology comprises a standard common-emitter amplifier but with the inclusion of a switch connected at the emitter terminal of the amplifier.**

The switched model of the proposed amplifier is obtained and the controller is implemented.

Finally, its behavior is simulated and its proper operation is verified.

Keywords—BJT, hysteresis controller, non-linear model, OP-AMP, switched amplifier.

I. INTRODUCTION

In the microelectronics field, one of the hot topics is the theory of low-power signal amplification. It can be noted, moreover, that there are many research papers associated with this area. To name a few [1]–[9]. One can do a short review of the existing literature and find that the amplification of these signals is carried out either by the typical bipolar junction transistor (BJT) or by the well-known and so typical operational amplifier (OP-Amp) [1]–[9]. The other types of devices such as the field effect transistors (JFETs and MOSFETs) are more commonly used for switching applications [10], and this reason, they are not included in amplifier applications. However, it is possible to note, that nowadays the trend is the use of OP-Amp in most amplifier applications, in the low to high-frequency range [11], [12]. Although there are still some applications where BJTs can be found in operation, such as in power amplifiers, to name, in short, the use of BJTs for amplification applications is becoming smaller.

Now, if focusing on applications where the voltage amplification at the output of a given amplifier, which operates at medium frequencies, it can be noted that, today, OP-Amps dominate the field [11], [12]. However, it can be noted that in this type of application, the amplification mechanisms are not regulated and depend directly on the resistors that are part of the bias circuit [11], [12]. Moreover, in the case of BJTs, the gain expression depends directly on the load resistor R_L, which is not often the case for OP-Amps. This dependence of the gain on the R_L can lead to problems in the regulation of the output voltage, due to typical disturbances occurring in R_L.

A simple way to overcome the drawback of gain dependence on R_L is related to a basic concept from control theory. Include a feedback loop of the output voltage and then compare it with the reference value of the voltage, generating an error signal, then be sent to a controller or compensator, which will generate a signal proportional to the effort of regulating the output voltage, which is finally sent to the actuator of the amplifier [13], [14]. The challenge in this instance, then, is to determine which would be the actuator and how it would operate in the amplifier.

In this work, a proposed topology of a switched amplifier with common-emitter variable voltage gain (CE-SA) is presented. The topology is described, then its dynamic modeling is presented, the controller and actuator chosen for the CE-SA are described, and finally, its behavior is simulated.

II. PROPOSED CE-SA TOPOLOGY

The proposed CE-SA topology is shown in Fig. 1. From Figure 1, this topology consists of an amplifier configured as a conventional common emitter [11], [12], where the BJT transistor Q_1, acting as the amplifier element of the circuit. On the other hand, the BJT transistor Q_2 operates as the switching element, performing in the saturation and cutoff regions [11], [12]. The proposed topology consists of the bias resistors R_1 and R_2, the collector resistor R_C and the emitter resistors R_E. The bias voltage is defined as V_{CC}. In the ac operating regime the C_C coupling capacitor connects to the circuit, the input stage, configured by a sinusoidal voltage source $v_i(t)$ and an inductor L operating as an input filter. The coupling capacitor C_B allows to connect the amplifier with the output stage comprised by a capacitor C operating as an output filter and the load resistor R_L. The pass capacitor C_E allows coupling Q_2 to the circuit, allowing switched operation. The currents $i_i(t)$, $i_C(t)$, $i_B(t)$, and $i_E(t)$ are the input, collector, base, and emitter currents respectively. The voltages $v_{BE}(t)$ and $v_{CE}(t)$ are the voltages

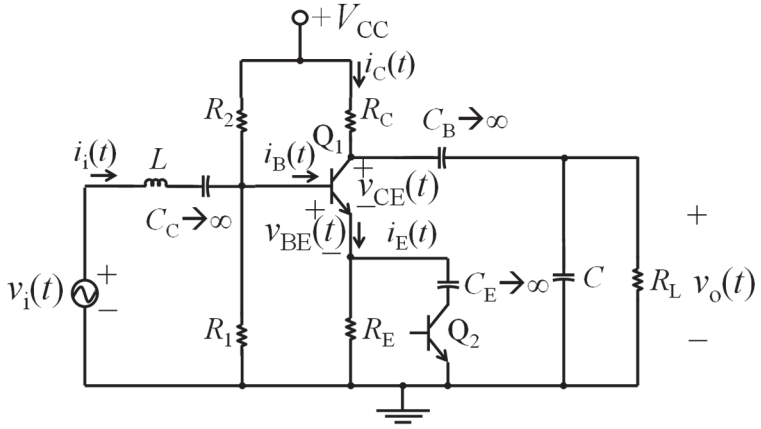

Fig. 1. Proposed topology of CE-SA.

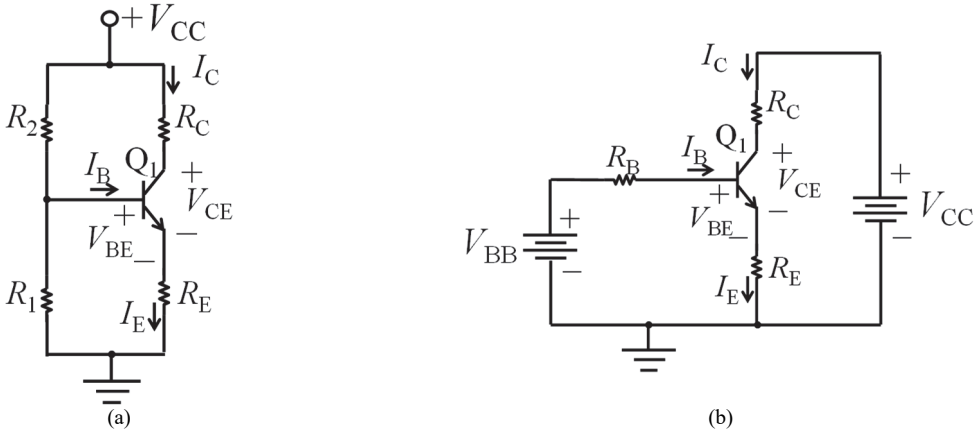

Fig. 2. CE-SA operating in dc regime. (a) Topology of the CE-SA in dc bias. The capacitors C_B, C_C, and C_E approach open circuits; (b) Topology of the CE-SA in dc bias with equivalent Thévenin input network.

measured between the base and emitter and between collector and emitter respectively. Finally, $v_o(t)$ is the output voltage.

III. Modeling of the CE-SA

In this section, the main equations of operation of the CE-SA will be presented, when it operates in dc and ac conditions. Q_1 is assumed to operate in the linear region.

A. Dc operation

During dc operation, the coupling capacitors and the pass capacitors, i.e. C_B, C_C, and C_E, respectively, approach open circuits, allowing to convert the topology described in Fig. 1, in a new circuit illustrated in Fig. 2(a), known as dc biased amplifier [11], [12]. From Fig. 2(a) a Thévenin equivalent circuit can be developed from the combination of resistors R_1, R_2 and source V_{CC}, obtaining a new CE-SA circuit for dc regime, described in Fig. 2(b) [11], [12]. Note in Fig. 2 the replacement of lower case letters by upper case letters, since it is assumed that the variables contain only dc components. The definitions of V_{BB} and R_B are presented in equations (1) and (2) respectively.

$$V_{BB} = \frac{R_B}{R_2} \cdot V_{CC} \tag{1}$$

$$R_B = R_1 || R_2. \tag{2}$$

Taking into account (1) and (2), Fig. 2(b) and [11], [12], for a maximum voltage output excursion $v_o(t)$, the operating point of the CE-SA are shown in (3) and (4).

$$V_{CE_Q} = \frac{1}{2} \cdot V_{CC} \tag{3}$$

$$I_{C_Q} = \frac{V_{BB} - V_{BE}}{\frac{R_B}{\beta} + R_E}, \tag{4}$$

where β is the amplification factor in dc [11]. Since it has been assumed that Q_1 works in the linear region, the expressions $I_{CQ} = \beta I_B$, $I_{EQ} \approx I_{CQ}$, and $V_{BE} = 0.7$ V are verified.

B. Ac operation

On operation of the CE-SA in ac regime, the C_C, C_B, and C_E capacitors are converted to short circuits. In addition, Q_1 is converted to itssmall-signal model

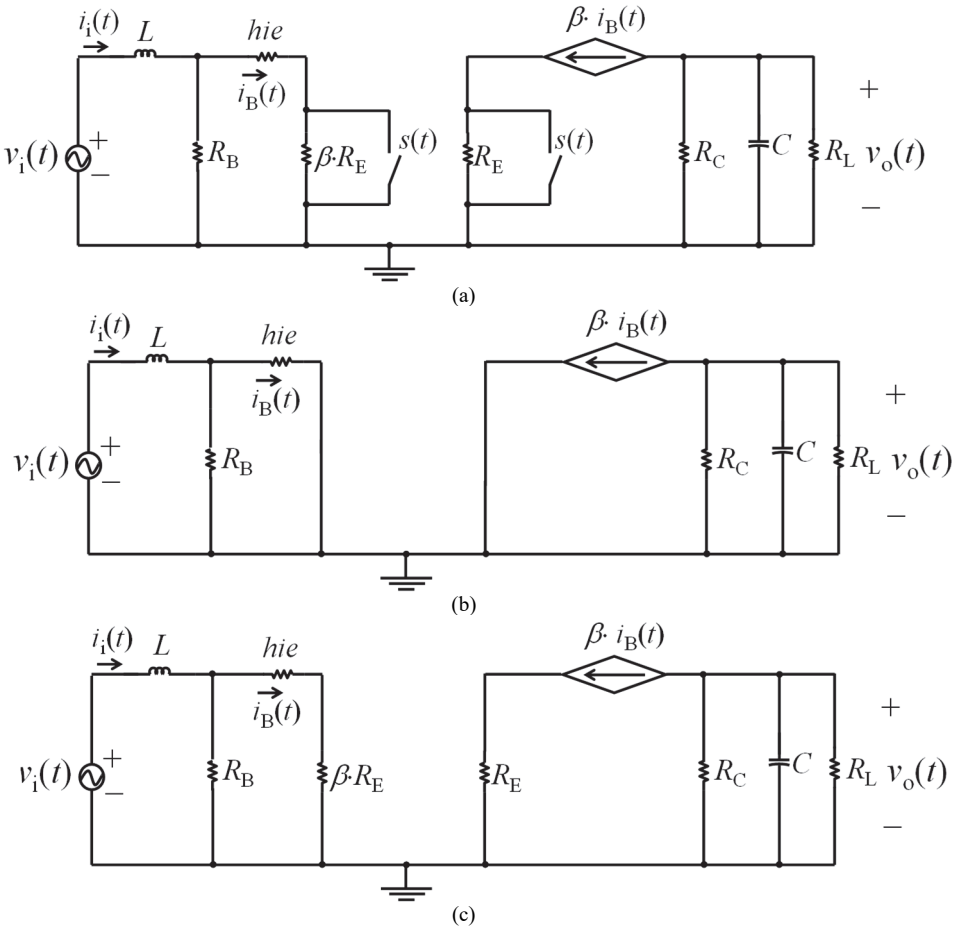

Fig. 3. CE-SA switching model for ac regime operation. (a) CE-SA switching model with the incorporation of the reflection of R_E and the switching function $s(t)$; (b) CE-SA switching model when $s(t)$ is on; (c) CE-SA switching model when $s(t)$ is off.

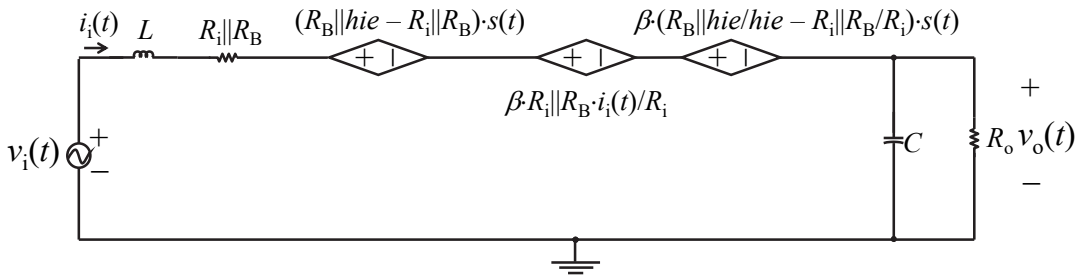

Fig. 4. Switched model of the CE-SA.

(Q_1 is assumed to operate in the linear region) and Q_2 is replaced by its equivalent corresponding switch $s(t)$ (Q_2 operates in the cut-off and saturation region). Thus, with these transformations of transistors Q_1 and Q_2, the switching model of the CE-SA for ac regime is depicted in Fig. 3(a). It should be noted that the switching model in Fig. 3(a) incorporates the analytical method of reflection of R_E and $s(t)$. The definition of the switching function $s(t)$ is given in (5).

$$s(t) = \begin{cases} 1, & Q_2 = \text{on} \\ 0, & Q_2 = \text{off} \end{cases} \tag{5}$$

Fig. 3(a) shows the switching model of the CE-SA when $s(t) = 1$. The state equations related to Fig. 3(a) are given in (6). From (6), *hie* and R_o are defined in (7) and (8) respectively.

$$hib = \frac{V_T}{I_{E_Q}},\ hie = \beta \cdot hib \tag{7}$$

$$R_o = R_C||R_L. \tag{8}$$

From (7), $V_T = 26$ mV is the thermal voltage; *hie* and *hib* are the hybrid parameters related to the input resistance of the small-signal model of Q_1, for the common-emitter and common-base configurations,

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{i}}(t) \\ v_{\mathrm{o}}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_{\mathrm{B}}||hie}{L} & 0 \\ -\beta\cdot\frac{R_{\mathrm{B}}||hie}{hie\cdot C} & -\frac{1}{R_{\mathrm{O}}\cdot C} \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{i}}(t) \\ v_{\mathrm{o}}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \cdot v_{\mathrm{i}}(t). \tag{6}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{i}}(t) \\ v_{\mathrm{o}}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_{\mathrm{i}}||R_{\mathrm{B}}}{L} & 0 \\ -\beta\cdot\frac{R_{\mathrm{i}}||R_{\mathrm{B}}}{R_{\mathrm{i}}\cdot C} & -\frac{1}{R_{\mathrm{O}}\cdot C} \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{i}}(t) \\ v_{\mathrm{o}}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \cdot v_{\mathrm{i}}(t). \tag{9}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{i}}(t) \\ v_{\mathrm{o}}(t) \end{bmatrix} = \begin{bmatrix} -\frac{\left(R_{\mathrm{i}}||R_{\mathrm{B}}+(R_{\mathrm{B}}||hie-R_{\mathrm{i}}||R_{\mathrm{B}})\cdot s(t)\right)}{L} & 0 \\ -\frac{\beta\cdot\left(\frac{R_{\mathrm{i}}||R_{\mathrm{B}}}{R_{\mathrm{i}}}+\left(\frac{R_{\mathrm{B}}||hie}{hie}-\frac{R_{\mathrm{i}}||R_{\mathrm{B}}}{R_{\mathrm{i}}}\right)\cdot s(t)\right)}{C} & -\frac{1}{R_{\mathrm{O}}\cdot C} \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{i}}(t) \\ v_{\mathrm{o}}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \cdot v_{\mathrm{i}}(t). \tag{10}$$

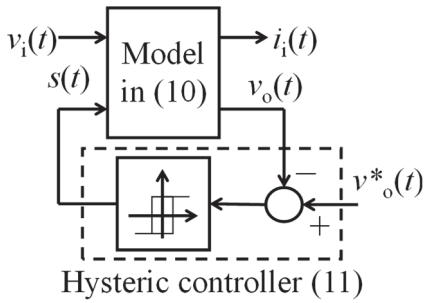

Fig. 5. Proposed control diagram.

respectively [11], [12]. On the other hand, Fig. 3(c) illustrates the switching model of the CE-SA in ac operation, when $s(t)$ = 0. The state equations representative of the model in Fig. 3(c) are shown in equation (9). From (9) $R_{\mathrm{i}} = hie + \beta \cdot R_{\mathrm{E}}$. Combining equations (6) and (9) and considering (5), the switching model of the CE-SA, expressed in terms of its state equations, is obtained and presented in (10).

Combining equations (6) and (9) and considering (5), the switching model of the CE-SA, expressed in terms of its state equations, is obtained and presented in (10). The equivalent switching circuit of the CE-SA is depicted in Fig. 4. Finally, from (10) it is observed that the output $v_{\mathrm{o}}(t)$ is negative, which is confirmed that this amplifier is inverting in terms of voltage gain, $A_{\mathrm{v}}(t) = v_{\mathrm{o}}(t)/v_{\mathrm{i}}(t)$ [11], [12].

IV. Control Strategy

The goal of the control of the CE-SA is to regulate the $A_{\mathrm{v}}(t)$. In other words, it is desired to have a controlled amplification of the system. An observation of the model in (10) shows that the model is not linear and discrete. Moreover, since the input is time-varying, even in steady state, it is not possible to use the Taylor series linearization method, and thus, finally, to apply the control techniques for linear and time-invariant systems. To overcome this drawback, hysteresis control will be applied, which is one of the control techniques applied to nonlinear systems [15]–[19]. The proposed control diagram is shown in Fig. 5. The proposed control algorithm is shown in (11).

```
if v_o(t) <= 0
    if e_vo(t)> 0.1
       s(t) = 0;
    elseif e_vo(t)< −0.1
       s(t) = 1;
    end
else
    if e_vo(t)> 0.1
       s(t) = 1;
    elseif e_vo(t)< −0.1
      s(t) = 0;
     end
end,                                    (11)
```

where $e_{\mathrm{vo}}(t) = v^*_{\mathrm{o}}(t) - v_{\mathrm{o}}(t)$. It can be seen from (11) that the hysteresis control is applied for both the positive and negative half-cycle of $v_{\mathrm{o}}(t)$, avoiding the generation of a steady-state error in both cycles [18], [19]. Practically speaking, when $v_{\mathrm{o}}(t)$ is in its positive half-cycle, and $e_{\mathrm{vo}}(t)$ is greater than 0.1, Q_2 is set to off if $e_{\mathrm{vo}}(t)$ is less than –0.1, Q_2 is set to on. On the other hand, when $v_{\mathrm{o}}(t)$ is in its negative half-cycle, if $e_{\mathrm{vo}}(t)$ is greater than 0.1, Q_2 is set to on and if $e_{\mathrm{vo}}(t)$ is less than –0.1, Q_2 is set to off.

V. Simulation Results

Fig. 6 presents the simulation results, which were obtained from the lossless model presented in Fig. 3 and modeled by (10), using MATLAB-Simulink. The simulation values are listed in Table 1. Fig. 6 presents the simulation results, which were obtained from the lossless model presented in Fig. 3 and modeled by (10), using MATLAB-Simulink.

The simulation values are listed in Table 1. The input signal is a sinusoidal voltage $v_{\mathrm{i}}(t)$ peak-to-peak voltage of 50 mV at a frequency f of 1 kHz and zero phase shift.

Fig. 6(a) and (b) show $v_{\mathrm{i}}(t)$ and the output voltage $v_{\mathrm{C}}(t)$ respectively. Fig. 6(c) and (d) show the input $i_{\mathrm{i}}(t)$ and base $i_{\mathrm{B}}(t)$ currents respectively, and finally, Fig. 6(e) and (f) depict the load resistance $R_{\mathrm{L}}(t)$ and the switching function $s(t)$ respectively.

Prior to system start-up, the initial output voltage $v_{\mathrm{C}}(t)$ is zero and the reference $v^*_{\mathrm{C}}(t)$ = -5 V peak-to-

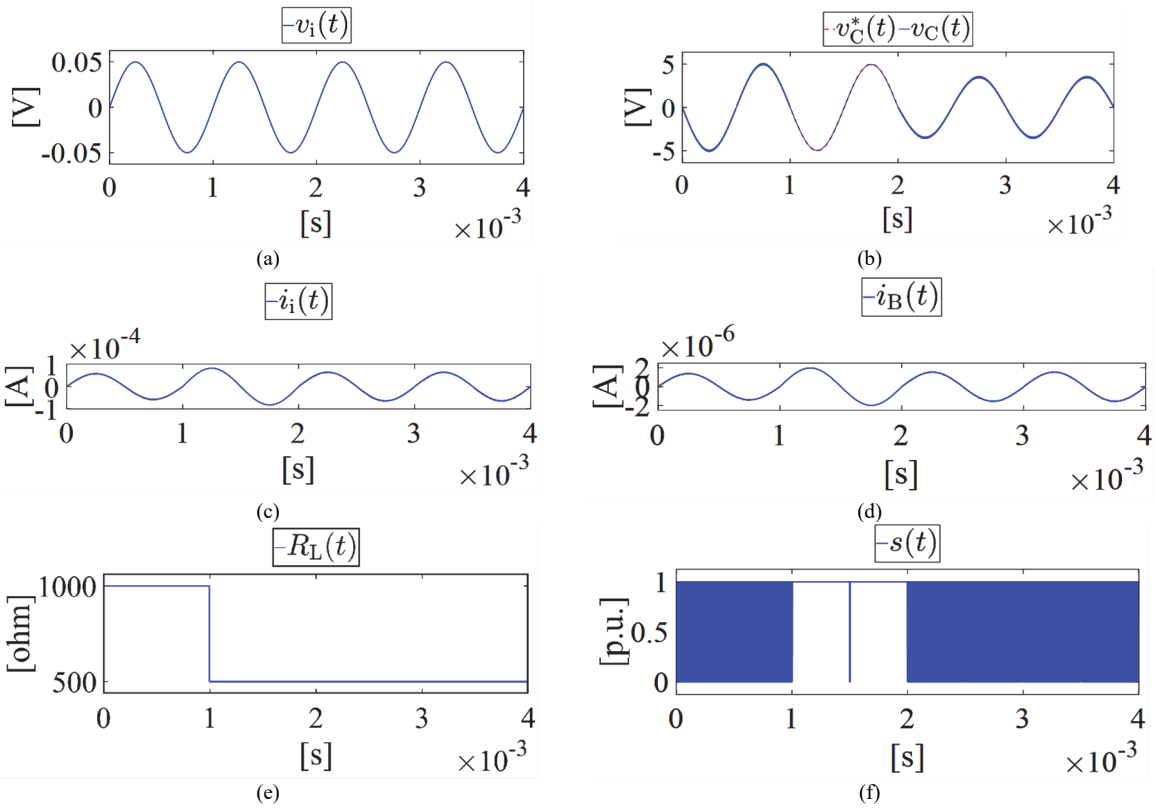

Fig. 6. Simulation results. Step changes in 1 ms and 2 ms in $R_L(t)$ and $v_o(t)$ respectively. (a) Input voltage $v_i(t)$; (b) Output voltage: reference $v^*_C(t)$ and measured $v_C(t)$; (c) Input current $i_i(t)$; (d) Base current $i_B(t)$; (e) Output resistance $R_L(t)$; and (f) Switching function associated with Q_2, i.e., $s(t)$.

peak. Then at start-up, $v_C(t)$ almost immediately reaches its reference, with a negligible error as seen in Fig. 6(b). From Fig. 6(e), at 1 ms, the CE-SA undergoes a perturbation represented by a step-change in the resistivity of R_L, which is modified from 1 kΩ to 0.5 kΩ, increasing $i_i(t)$ from 0.056 mA to 0.085 mA in order to maintain stable control of $v_C(t)$. A further consequence of this perturbation is the increase of $i_B(t)$ from 1.25 uA to 1.85 uA (see Fig. 6(d)) due to the direct relationship between $i_i(t)$ and $i_B(t)$.

Finally, and according to Fig. 6(f), Q_2 remains fixed in the conduction state, i.e., $s(t) = 1$, setting the CE-SA in the topology (see Fig. 3(c)) in which, $A_v(t)$ is the maximum (R_E is bypassed). It is also interesting to note, that between the time range 1 ms ≤ t < 2 ms the high-frequency ripple shown in $v_C(t)$ in Fig. 6(b), following hysteresis control, disappears.

TABLE 1. CE-SA PARAMETERS

Parameters	Values
R_1	3 kΩ
R_2	15 kΩ
R_C	2 kΩ
R_E	0.5 kΩ
R_L	1 kΩ
L	1 µH
C	0.5 pF
V_{CC}	24 V
β	200

At the same time, at 1.5 ms, it undergoes a very fast transition going from 1 to 0 and then to 1 again. At 2 ms and according to Fig. 6(b), the reference $v^*_C(t)$ changes from −5V peak-to-peak to −3.5 V peak-to-peak (step change), $v_C(t)$ reaching the reference value nearly instantly, displaying a negligible steady-state error. As is evident from Fig. 6(c) and (d), $i_i(t)$ and $i_B(t)$ change their values in order to keep $v_C(t)$ stable. Moreover, Q_2 switches back, evidencing the correct operation of $s(t)$ via the hysteresis control (see Fig. 6(f)).

Overall, the hysteresis control system operates correctly and shows a fast response to the R_L perturbation and to the step change of $v_C(t)$, showing negligible steady-state errors. It is also observed that the input voltage does not suffer any variation, thus proving the robustness of the CE-SA.

VI. CONCLUSION

A switched amplifier in common-emitter configuration, and with a regulated voltage gain has been proposed in this work.

A switched amplifier model has also been obtained, based on the system state variables, i.e., $i_i(t)$ and $v_C(t)$.

A simple hysteresis control has been implemented in order to regulate the output voltage $v_C(t)$ according to a reference $v^*_C(t)$.

Overall, it can be seen that the system operates properly, keeping the output voltage $v_C(t)$ stable despite the step change in R_L (disturbance) generated in the amplifier. This is an indication of the robustness of the system when using hysteresis control. Regarding the reference $v^*_C(t)$, it can be observed that $v_C(t)$ follows its reference quite well, presenting negligible errors. Moreover, independent of the change in R_L and $v^*_C(t)$, the input voltage $v_i(t)$ does not suffer any change, keeping its peak-to-peak value during the whole simulation time.

REFERENCES

[1] B. Perez-Verdu, J. L. Huertas, and A. Rodriguez-Vazquez, 'A new nonlinear time-domain op-amp macromodel using threshold functions and digitally controlled network elements', *IEEE Journal of Solid-State Circuits*, vol. 23, no. 4, pp. 959–971, Aug. 1988, doi: 10.1109/4.347.

[2] D. F. Bowers, 'A fast precision operational amplifier featuring two separate control loops', in *2014 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sep. 2014, pp. 72–75. doi: 10.1109/BCTM.2014.6981288.

[3] M. Gilasgar, A. Barlabé, and L. Pradell, 'High-Efficiency Reconfigurable Dual-Band Class-F Power Amplifier With Harmonic Control Network Using MEMS', *IEEE Microwave and Wireless Components Letters*, vol. 30, no. 7, pp. 677–680, Jul. 2020, doi: 10.1109/LMWC.2020.2994373.

[4] S. E. Hosseini and H. G. Dehrizi, 'A new BJT-transistor with ability of controlling current gain', in *International Multi-Conference on Systems, Signals & Devices*, Mar. 2012, pp. 1–4. doi: 10.1109/SSD.2012.6198085.

[5] K.-J. De Langen and J. H. Huijsing, 'Compact low-voltage power-efficient operational amplifier cells for VLSI', *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1482–1496, Oct. 1998, doi: 10.1109/4.720394.

[6] L. Kong *et al.*, 'Design of a Wideband Variable-Gain Amplifier With Self-Compensated Transistor for Accurate dB-Linear Characteristic in 65 nm CMOS Technology', *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 12, pp. 4187–4198, Dec. 2020, doi: 10.1109/TCSI.2020.2995725.

[7] I. M. Pandiev and E. Ch. Stoimenov, 'Development of Single-Transistor Amplifier Modular Laboratory Kits for Electronic Engineering Education', in *2020 XI National Conference with International Participation (ELECTRONICA)*, Jul. 2020, pp. 1–4. doi: 10.1109/ELECTRONICA50406.2020.9305170.[8]

F. A. Farag and Y. A. Khalaf, 'Digitally-Controlled Variable-Gain-Amplifier based on current conveyor with opamp and inverters only', in *2010 International Conference on Microelectronics*, Dec. 2010, pp. 224–227. doi: 10.1109/ICM.2010.5696123.

[9] D. G. Makarov, V. V. Kryzhanovskyi, V. G. Krizhanovski, and A. V. Grebennikov, 'Experimental investigation of class E power amplifier with shunt filter for reduced duty ratio', in *2018 International Conference on Information and Telecommunication Technologies and Radio Electronics (UkrMiCo)*, Sep. 2018, pp. 1–4. doi: 10.1109/UkrMiCo43733.2018.9047572.

[10] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, Mass, 2001.

[11] C. J. Savant, M. S. Roden, and G. L. Carpenter, *Electronic Design: Circuits and Systems*, Subsequent edition. Redwood City, Calif: Benjamin-Cummings Pub Co, 1990.

[12] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. Oxford University Press, 2004.

[13] O. Katsuhiko, *Modern Control Engineering*. Boston, 2009.

[14] *The Control Handbook (three volume set)*. CRC Press, 2018. doi: 10.1201/9781315218694.

[15] A. Dwivedi, 'Analysis of Hysteresis current controllers for Three-Phase PWM Rectifier: A Survey', Apr. 2015.

[16] Krismadinata, N. A. Rahim, and J. Selvaraj, 'Implementation of Hysteresis Current Control for Single-Phase Grid Connected Inverter', in *2007 7th International Conference on Power Electronics and Drive Systems*, Nov. 2007, pp. 1097–1101. doi: 10.1109/PEDS.2007.4487841..[17] A. Patel *et al.*, 'Multi-secondary transformer: A modeling technique for simulation - II', in *2013 International Conference on Electrical Machines and Systems (ICEMS)*, Oct. 2013, pp. 2271–2274. doi: 10.1109/ICEMS.2013.6754564.

[18] H. Khalil, *Nonlinear Control*, 1st edition. Boston: Pearson, 2014.

[19] J.-J. Slotine and W. Li, *Applied Nonlinear Control: International Edition*. Englewood Cliffs, NJ, 1990.